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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/241,695	02/02/1999	AKIHARU MIYANAGA	SEL123	9049

7590 01/29/2003

COOK MCFARRON & MANZO
200 WEST ADAMS STREET
SUITE 2850
CHICAGO, IL 60606

EXAMINER	
HU, SHOUXIANG	
ART UNIT	**PAPER NUMBER**
2811	

DATE MAILED: 01/29/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/241,695	MIYANAGA ET AL.	
	Examiner	Art Unit	
	Shouxiang Hu	2811	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *08 November 2002* .

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,3,5-13,15-48 and 50-59* is/are pending in the application.

4a) Of the above claim(s) *5-13,16,17,19,20,22,23,25,26,35-41 and 50-55* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,3,15,18,21,24,27-34,42-48 and 56-59* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Claim Objections

1. Claims 1, 3, 15, 18, 21, 24, 27-34 and 42-48 are rejected to because of the following informalities and/or defects:

Claims 1, 3, 15, 18, 21, 24, 27-34 and 42-48 recite the combined subject matters that the impurity region being formed under both of the channel forming region and the source region, and that a concentration of the second impurity in the channel forming region is from 1/100 to 1/10 of that in the impurity region; but they fail to definitely define the meaning and/or scope of the recited term "that in the impurity region" therein, as to whether it means the concentration of the second impurity in the portion of the impurity region underlying the source region or in the portion of the impurity region underlying the channel forming region. According to the original disclosure, the concentration in the impurity region is not uniform (see page 9, lie 26, through page 10, line 1); and the original specification only prefers that the concentration of the second impurity in the channel forming region is from 1/100 to 1/10 of that in the portion of the impurity region underlying the channel forming region, i.e., the concentration of in punch through stopper region (see page 10, lines22-28).

Appropriate correction is required.

Claim Rejections - 35 USC § 112

2. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

Claim 3 is rejected under 35 U.S.C. 112, first paragraph, as containing subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention. Claim 3 recites the subject matter that the impurity region is not in contact with the source/drain region, no support for this recited subject mater is found in the original disclosure (see the overlapping between the source/drain region (302 or 303) and the impurity region (305) in Fig. 3), given the new definition for the impurity region in the amended claim 1, which now also includes the impurity region (see region 305 in Fig. 3, or region 804 in Fig. 8) formed under the source region.

3. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claim 57 recites the limitations "the first n-type impurity", "the second n-type impurity" and "the first and the second p-type impurity(ies)." There is insufficient antecedent basis for each of those limitations in the claim.

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 1, 3, 15, 18, 21, 24 and 27-34, insofar as being in compliance with 35 U.S.C. 112 and as being best understood in view of the claim objections above, are rejected under 35 U.S.C. 103(a) as being unpatentable over Chen et al. ("Chen"; US 5,926,712) in view of Ko et al. ("Ko"; 5,686,321).

Chen discloses a semiconductor IC device including MOSFETs (see col. 1, lines 11-19), each comprising (see Figs. 2(a)-2(f)): source and drain regions (219; n+) with a first impurity; a channel forming region between the source and drain regions (a top portion of the p-type silicon substrate); an impurity region (217; p type, including a punchthrough stop region under the channel forming region) including a second impurity having a conductive type opposite to that of the source and drain regions and being formed under both of the channel forming region and the source region; and a pair of LDD regions (see the n- regions in Fig. 2(f)).

Although Chen dos not explicitly discloses that the concentration of the second impurity in the channel forming region is from 1/100 to 1/10 of that in the portion of the impurity region underlying the channel forming region, one of ordinary skill in the art would readily recognize that the impurity concentrations of the channel forming regions and the punchthrough stop region are well recognized parameters of importance subject to routine experimentation and optimization; and that a channel forming region can normally have a doping concentration of $5x10^{16}$ /cm^3 through $1x10^{17}$ /cm^3 and a punchthrough stopper region can normally have a doping concentration of $1x10^{18}$ /cm^3

through $1x10^{19}$ /cm^3, for effectively prevent punchthrough, as evidenced in Ko. Ko teaches (Fig. 1-4; and see col. 4, lines 1-11) that it is desirable to form the channel forming region (63) with a doping concentration range that covers $5x10^{16}$ /cm^3 through $1x10^{17}$ /cm^3 and to form the punchthrough stopper region (24) with a doping concentration range that covers $1x10^{18}$ /cm^3 through $1x10^{19}$ /cm^3, which therefore covers a concentration ratio that is between 1/100 and 1/10.

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to make the semiconductor device of Chen with the concentration of the impurity in the channel forming region being from 1/100 to 1/10 of that in the portion of the impurity region underlying the channel forming region, as taught in Ko, so that a semiconductor device with increased punchthrough voltage would be achieved.

Regarding claims 18, 21, 24 and 29-33, it is noted that it is old and well known in the art that semiconductor devices having MOSFETs with short channels can be used in various well-known devices with different functionalities, including microprocessors (such as RISC or ASIC ones), cellular phones, personal handy phone systems and portable computers (as evidenced in the prior art references such as Rostoker et al. (US 5,563,928; see co.3, lines 52-58) and Okumura et al. (US 5,945,972; see col. 2, lines 15-21)). Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to make the semiconductor device and to use it in the above well-known devices for achieving desired device functionalities with improved performance.

Regarding claim 27 and 34, it is noted that one of ordinary skill in the art would readily recognize that the punchthrough region can be formed at a depth of about 150 nm, as evidenced also in Ko, which further discloses that the peak impurity region can be formed at a depth of about 150 nm (col. 4, lines 8-9).

Regarding claim 28, it is noted that the MOSFET in Chen is a bulk MOSFET formed on a silicon substrate, and one of ordinary skill in the art would readily recognize that such a silicon substrate with the bulk MOSFET device is commonly formed of a single crystal silicon wafer.

6. Claims 42-48 are rejected under 35 U.S.C. 103(a) as being unpatentable over Chen et al. ("Chen"; US 5,926,712) in view of Ko et al. ("Ko"; 5,686,321), as applied to claims 1, 3, 15, 18, 21, 24 and 27-34 above, and further in view of Chang et al. ("Chang"; US 5,893,740).

The disclosure of Chen and Ko are disclosed as applied to claims 1, 3, 15, 18, 21, 24 and 27-34 above.

The device disclosed in Fig. 2(f) in Chen is an n-channel MOSFET.

Although Chen and Ko do not expressly disclose that the device can further comprise a p-channel MOSFET so as to form a CMOS circuit, one of ordinary skill in the art would readily recognize that CMOS structure is one of the most common basic structures in an IC device for achieving advanced functionality with reduced power consumption, and that a CMOS structure can be readily formed with an n-channel MOSFET and a p-channel MOSFET having a polarity opposite to that of the n-channel

MOSFET, as evidenced in Chang (see col. 5, lines 6-7, col. 2, lines 59-61, and col. 3, lines 65-67, wherein the p-channel MOSFET (Figs. 1A-1C), comprising: second source/drain regions (16; p+ with B); a second channel forming region (between the LDD regions 14); and a second impurity region including a second n-type impurity (18, Ar or P), forming a reversed polarity as compared with that of the corresponding regions in the n-channel MOSFET (see Figs. 3A-3C)).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to make the above semiconductor device collectively taught by Chen and Ko and further incorporate a p-channel MOSFET having a reverse polarity to the n-channel MOSFET, as taught in Chang, so that a CMOS semiconductor device having advanced functionality with reduced power consumption would be achieved.

Regarding claim 43, it is noted that Ar and P are the two most commonly used n-type impurities, B is most commonly used p-type impurity in the industry, as evidenced also in Chang (see col. 3, lines 51-54, and lines 21-22, respectively).

7. Claims 56-59 are rejected under 35 U.S.C. 103(a) as being unpatentable over Chen et al. ("Chen"; US 5,926,712) in view of Ko et al. ("Ko"; 5,686,321), as applied to claims 1, 3, 15, 18, 21, 24 and 27-34 above, and further in view of Mikoshiba (JP 56060061 A) and/or Okumura et al. ("Okumura"; US 5,945,972).

The disclosure of Chen and Ko are disclosed as applied to claims 1, 3, 15, 18, 21, 24 and 27-34 above.

Chen further discloses that, as illustrated by the arrow direction shown in Fig. 2(d), the second impurity for the punchthrough stop region is injected along a direction of substantially about 45 degrees to the vertical. And, it is noted that the exact impurity injection direction is a well recognized parameter of importance subject to routine experimentation and optimization. Although Chen and Ko do not expressly disclose that the channel is oriented along a <100> direction, one of ordinary skill in the art would also readily recognize that the channel in a MOSFET can be desirably aligned to a <100> crystal direction on a wafer parallel to a (100) crystal plane for minimizing the adverse piezo effect, as evidenced in Mikoshiba (Fig. 1), which comprises a gate (5) aligned along a {100} direction on a (100) substrate. With the impurity injection direction being about 45-degrees to the vertical and the channel being aligned along a <100> direction, the impurity injection direction would be inherently along a <110> direction.

In addition, although Chen and Ko do not expressly disclose that the MOSFET device can be used as an EL display device, one of ordinary skill in the art would readily recognize that a MOSFET can be readily used in EL display units having an actively-addressed structure for good display quality, as evidenced in Okumura (see col. 28, lines 14-11).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to make the above semiconductor device collectively taught by Chen and Ko with the channel being aligned to a <100> crystal direction on a wafer parallel to a (100) crystal plane, and with the MOSFET being applied to an EL display device, as taught in Mikoshiba and/or Okumura, so that a desired EL display

device with increased punchthrough voltage and minimized piezo effect would be achieved. And, in such a device collectively taught by Chen, Ko, Mikoshiba and Okumura, the impurity injection direction is about 45-degrees to the vertical and the channel is aligned along a <100> direction; thus the second impurity injection direction would be inherently along a <110> direction, which would then be inherently perpendicular to a plane having the smallest atomic density of the semiconductor substrate.

Response to Arguments

8. Applicant's arguments with respect to claims 1, 3, 15, 18, 21, 24, 27-34 and 42-48 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. References C is cited as being related to a microprocessor with ASIC.

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Shouxiang Hu whose telephone number is (703) 306-5729. The examiner can normally be reached on Monday through Thursday, 7:30 AM to 6:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tom Thomas can be reached on (703) 308-2772. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 872-9318 for regular communications and (703) 872-9319 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or

proceeding should be directed to the receptionist whose telephone number is (703) 308-0956.

SH
January 24, 2003

Shouxiang Hu
Patent Examiner
TC2800